Selective and Atomic Scale Processes for Advanced Semiconductor Manufacturing

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Abstract: Continued device density scaling according to Moore's Law has resulted in the adoption of 3D device geometries and architectures and driven critical dimensions down to atomic scales. This tutorial briefly reviews the trends in device scaling since Dennard-style linear shrinking became untenable and outlines the forces driving 3D integration going forward as well as the impact these changes are having on manufacturing process technologies. The tutorial then introduces multi-patterning and atomic scale process technologies used for 10nm and beyond semiconductor manufacturing including plasma and thermal atomic layer deposition (ALD) and atomic layer etching (ALE) technologies. Selective processing including area selective deposition (ASD) is explained as an emerging technology enabling new device nodes and integration schemes. The scope of the discussion includes examples of how these technologies enable self-aligned and sub-lithographic patterning, and device and interconnect engineering along with EUV lithography to overcome edge placement error effects and realize atomic scale process control for manufacturing. Finally, a view of how integrated circuit manufacturing will continue to evolve through 3D monolithic and heterogeneous integration is presented to frame the future opportunities and challenges for advanced process technologies.

BIO: Robert D. Clark, Ph.D. is a Sr. Member of the Technical Staff at Tokyo Electron (TEL) working for the TEL Technology Center, America, LLC. He joined TEL in 2006 and worked in Albany, NY to develop advanced Atomic Layer Deposition (ALD) processes for high k dielectrics used in logic and memory devices. In 2010 he relocated to Silicon Valley and was elected Member of the Technical Staff, and in 2015 he was elected Sr. Member of the Technical. His research focuses on thin film process technologies for advanced and emerging devices, materials, and interconnect structures for use in semiconductor manufacturing. Dr. Clark has contributed to multiple processes for advanced CMOS contacts and high k and metal gate structures used currently in advanced semiconductor logic and memory device manufacturing.

Prior to joining Tokyo Electron, Dr. Clark completed his Ph.D. in Chemistry at the University of California, Irvine in 2000 and B.S. and M.S. degrees in Chemistry at Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA, USA in 1993 and 1995 respectively. From 2000-2006 Dr. Clark was a Principal Research Chemist for Air Products and Chemicals, Inc. (APCI) at the Schumacher site in Carlsbad, CA. At APCI Dr. Clark was the lead technologist for the development of high k and metal gate precursors where he helped to develop the first precursor used for ALD high k gate dielectrics in CMOS manufacturing.

Dr. Clark has served previously as the science advisory committee chair for SRC device sciences and received a 2017 SRC Mahboob Khan outstanding industrial liaison award. He currently contributes to the SRC Decadal Plan executive committee and is a member of multiple conference committees including the AVS ALD, AVS ASD, and VLSI-TSA conference committees. At TEL he has been a U.S. employee of the year, and in 2018 received the most impactful patent award for the U.S. as well. He currently holds more than 110 issued patents worldwide and has authored or co-authored hundreds of journal and conference publications including numerous invited talks and articles.