## Interconnect Resistivity: New Materials Daniel Gall, Rensselaer Polytechnic Institute

**Abstract:** A major challenge for the continued downscaling of integrated circuits is the resistivity increase of Cu interconnect lines with decreasing dimensions, limiting power efficiency and causing the interconnect delay to exceed the gate delay. This resistivity increase is due to electron scattering at Cu surfaces and grain boundaries and leads to, for example, a 10-fold resistance increase for 10-nm-wide Cu lines. Alternative interconnect materials have the potential to outperform Cu. These include metals with a small electron mean free path to render electron scattering at surfaces and grain boundaries negligible, 2D materials as new liner/barrier layers which maximize the conductor cross-sectional area and facilitate specular surface scattering, and topological metals with protected surface states that suppress electron scattering. This talk presents recent research results focusing on these new materials for high-conductivity narrow interconnects.

**Daniel Gall** is a Professor of Materials Science and Engineering at Rensselaer Polytechnic Institute. He received his MS and PhD degrees in physics from the University of Basel and the University of Illinois. His research focuses on thin film deposition, the epitaxial growth of transition metal nitrides and metals, and their electronic structure and nanoscale electron transport. He has served as Assistant and Associated Editor for the Journal of Vacuum Science and Technology and Thin Solid Films, as chair of the AVS Advanced Surface Engineering Division and as program chair of the AVS International Symposium. Gall wrote over 170 peer-reviewed journal articles, presented his research at 80 invited lectures, and received the Alfred Geisler Memorial Award, NSF CAREER Award, IBM Faculty Award, LAM Research Award, and Bill Sproul Award. His students won over 60 poster competitions and best paper awards.